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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,832	07/21/2003	Steven P. Young	X-1335 US	6570

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,832	YOUNG, STEVEN P.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23-28,35 and 36* is/are allowed.

6)☒ Claim(s) *1-18,20,21 and 29-34* is/are rejected.

7)☒ Claim(s) *19 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/21/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation recites "IC" is vague. Clarification is required.

3. Claim 20 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The method claim 20 is dependent of apparatus claim.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-18, 20-21, 29-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Jones (6,563,340).

1. Jones shows a multi-chip device (Fig. 1, 2, 6) comprising:

a group of aligned regions (CL, Fig. 6), each region having a programmable interconnection (152B); a first IC (104C) having a first region of the group of aligned regions;

a second IC (106C) having a second region of the group of aligned regions; and

a supporting structure (102C) having one or more signal lines (152B between 116C and 120C, Fig. 6 or 112, Fig. 1, col. 2, lines 15-20), wherein the first region is directly connected to the second region via one of the signal lines.

2. Jones shows the supporting structure comprises a carrier die (col. 3, line 1).

3. Jones shows each region further comprises programmable logic (CPLD).

4. Jones shows wherein each region of the group of aligned regions on the first IC is substantially identical (3 CL in each column).

5. Jones shows each region of the group of aligned regions on the second IC is substantially identical (3 CL in each column).

6. Jones shows the first region includes a line driver and a pad, the pad configured to connect the first region to the second region (col. 2, lines 25-29).

7. Jones shows the second region includes a tile (CL) of a field programmable gate array.

8. Jones shows a multi-chip module having: a first die (104C, Fig. 6; die, col. 1, lines 10-12) having a first column of a first plurality of tiles (CL in the first row is considered a tile, CL in the middle row is considered a tile, CL & I/O bank is consider another tile), wherein each tile of the first plurality includes programmable logic (programmable logic cluster); a second die (106C) having a second column of a second

plurality of tiles (CL), wherein the second column is aligned with the first column; and a supporting substrate (102C) having a plurality of signal lines (152B between 116C and 120C), wherein a tile (a bottom CL of die 104C with I/O bank is considered a tile) in the first column is directly connected to a tile (a top CL of die 106C with I/O bank is considered a tile) in the second column via one of the plurality of signal lines.

9. Jones shows wherein the tile in the first column comprises a logic block (CL) and a switching block (I/O block).

10. Jones shows the tile in the first column further comprises a line driver and a pad, the pad configured to connect the tile in the first column to the tile in the second column (col. 2, lines 25-29).

11-14. Jones shows the dies are identical or heterogeneous (col. 4, lines 15-20).

15. Jones shows first die has programmable logic and the second die has programmable logic and an embedded application specific integrated circuit (107A, Fig. 2).

16. Jones shows the ASIC is selected from a group consisting of a microprocessor, a digital signal processor, and an arithmetic processing module (col. 3, lines 51-59).

The apparatus above is applicable to the method claims 17-18, 20.

21. Jones shows multi-chip module, having programmable interconnections, comprising; means for arranging a first plurality of substantially identical connected regions (Two columns of CL and I/O bank are considered as one region) on a first

integrated circuit (104C); means for arranging a second plurality of substantially identical connected regions on a second IC; and means (152B between 116C & 120C) for connecting a first region in the first plurality to a second region in the second plurality.

29. Jones shows a system having a plurality of dice, the system comprising: a first die (104C) of the plurality of dice, comprising first input/output blocks (I/O banks on the left and the right) for communicating with circuits located outside of the first die, and a first function block (two columns of CL and I/O bank at the bottom) connected to a first interconnect line (152B); a second die of the plurality of dice (106C), comprising second input/output blocks (I/O banks on the left and the right) for communicating with circuits located outside of the second die, and a second function block (two columns of CL and I/O bank at the top) connected to a second interconnect line (152B); and a signal line connecting the first interconnect line to the second interconnect line (152B between 116C & 120C), wherein a signal propagates from the first interconnect line to the second interconnect line without propagating through any of the first input/output blocks of the first die.

30. Jones shows the signal does not propagate through any of the second input/output blocks of the second die (the signal propagate through the I/O bank bottom of 104C and the top I/O bank of 106C).

31. Jones shows the first function block is connected to the second function block via the signal.

32-34. The limitations of claims 32-34 are rejected as above.

Allowable Subject Matter

3. Claims 19, 22, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 23-28, 35-36 are allowed.

5. The following is an examiner's statement of reasons for allowance: with respect to claims 23, 35, in addition to other limitations of claims, the prior art fails to teach or discloses the applicant's invention as claimed, particularly the feature describing:

- each element in the first column connected to each element in the second column by the signal lines.
- First to fourth interconnection points.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Reddy (5,767,565) discloses a plurality of dice having programmable logic and interconnection and multiple device are interconnected through interconnected scheme.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anh Q. Tran
Examiner
Art Unit 2819

12/6/04